Remarks/Arguments:

In response to the various paragraphs of the Office Action, Applicants offer the following remarks.

Claim To Right of Priority

The Examiner in the Office Action Summary has acknowledged the claim for foreign priority. The Examiner indicates that certified copies of the priority documents have been received. The Examiner, however, has inadvertently acknowledged box (b) which is "Some". Applicants request that the Examiner acknowledge box (a) which is "All".

Preliminary Amendment of 12/04/01

The Examiner has indicated that the Preliminary Amendment, filed on December 4, 2001, is ambiguous and, therefore, has not been entered. Accordingly, Applicants are now providing the same amendments, previously made to the specification, with this Response to the Office Action. Applicants request that the Examiner enter these, as amendments to the specification.

Drawings

As requested, Figure 9 and Figure 10 have now been designated with a legend of --Prior Art--.

Specification

As requested, a new abstract is enclosed.

As requested, Applicants have now also amended pages 2 and 15 of the specification.

Claim Objections

Applicants have now amended claim 6, as suggested by the Examiner.

Section 112 Rejections

As requested, claims 2 and 5 have been amended, by reciting that "N" is a positive integer.

Section 103 Rejections

Claims 1 and 4 have been rejected as being obvious in view of Graef, Yu and Brauch. In addition, claims 2, 3, 5 and 6 have been rejected as being obvious in view of Graef, Yu, Brauch, Bastiani and Applicants' admitted prior art (APA). Applicants respectfully submit that these rejections are overcome for the reasons set forth below.

Applicants' invention, as recited in amended claim 1, includes features which are not anticipated or suggested by the cited references, namely:

- asynchronous reading and writing means of reading a predetermined amount of data from and of writing the predetermined amount of data into the memory on a first-in-first-out basis, **the predetermined amount of data including a plurality of words stored in a respective plurality of address locations of the memory**;
- an error write counter of counting counts up by 1 **for each word of the plurality of words containing an error flag that is written into the respective plurality of address locations**;

- an error read counter of counting up by 1 **for each word of the plurality of words containing an error flag that is read from the respective plurality of address locations**;

- comparing means of comparing a value of the error write counter with a value of the error read counter, the comparing means outputting a logic level of 0 when the value of the error write counter is coincident with the value of the error read counter, and the comparing means outputting a logic level of 1 if the former value is different from the latter value, **wherein the logic level of 1 indicates at least one error flag is set in the plurality of words stored in the respective plurality of address locations**.

Basis for the features of amended claim 1 may be seen, for example, in Figure 1. As shown, memory 23 includes a predetermined amount of data, including 8 words, each word stored in a different address location. Basis for each word of the plurality of words containing an error flag may be seen, for example, in Figure 9. As shown, the word includes a parity error and a forwarding error. Basis for the comparing means comparing a value of the error write counter with a value of the error read counter may be seen in Figure 1, for example. As shown, error comparing circuit 63 compares a value of error write counter 61 with a value of error read counter 62. Basis for the comparing means outputting a logic level of 1 indicating that at least one error flag is set in the plurality of words stored in the memory may be found in the specification, for example, at page 23, bottom paragraph, to page 24, line 4. As described, the error comparing circuit becomes a logic level 1 (the LSR7 bit), if at least one error flag having a logic level of 1 exists

in memory 23; and becomes a logic level 0, if an error flag of a logic level of 1 does not exist in memory 23.

As also described in the specification, for example, at page 2, lines 2-25, the LSR7 bit indicates whether at least one error flag is set to a logic level 1 in a receiver FIFO. The LSR7 is the logical sum of all of columns that correspond to error flags of respective words stored in the receiver FIFO. If the number of words of the receiver FIFO are increased, it becomes more difficult to configure the output of the LSR7 bit. When the number of words are increased, output lines must also be increased to independently read each of the columns corresponding to the error flags of each word. This, in turn, increases the chip area and the number of logic gates required. The present invention, as recited in amended claim 1, advantageously avoids these problems.

Graef discloses a comparator circuit that monitors the write blocks with the read blocks, in order to determine whether buffers can accept data and transmit data. Graef discloses flag registers 14-17 that indicate whether the buffers are almost empty, empty, almost full, or full. Graef, however, does **not** disclose or suggest a **comparator which compares a value of an error write counter with a value of an error read counter**. Graef does **not** disclose or suggest **outputting a logic level of 0 when the value of the error write counter is coincident with the value of the error read counter**. Graef does **not** disclose **outputting a logic level of 1 when the former value is different from the latter value**. Furthermore, Graef does **not** disclose or suggest outputting the logic level of 1, **so that it indicates that at least one error flag is set in the words stored in memory**.

Yu discloses a FIFO system for performance monitoring to record and count errors in a receive FIFO and a transmit FIFO. Yu discloses a performance monitor that uses an error counter to count the number of errors in the transmit FIFO. Yu, however, does **not** suggest **comparing errors counted in the transmit FIFO with errors counted in the receive FIFO**. Furthermore, Yu does **not** suggest **providing an output from the comparator, wherein a logic level of 1 indicates that at least one error flag is set in the words stored in memory**.

Brauch discloses a method for locating defects on a chip. Brauch discloses writing a known data value into a memory and reading back the same data value from the memory. If there is a discrepancy between the data read and the data written, Brauch discloses providing a logic level of 1 to the user. Brauch, however, does **not** disclose **writing words into memory wherein each word contains an error flag**. Brauch does **not** disclose **counters that count error words containing an error flag.** Brauch does **not** disclose a **comparator that compares the number of words containing an error flag counted by each counter**. Brauch also does **not** disclose **providing a logic level of 1 to indicate that at least one error flag is set in these words stored in the memory**. It is respectfully submitted that when Brauch provides a logic level of 1 as an output, that output merely indicates that a specific word, stored in a specific address, is **not** the same as a word read out from that same specific address. Thus, Brauch's comparison of two words is completely different from Applicants' invention of **a comparison to indicate at least one error flag is set in the data words stored in memory**.

Bastiani discloses a FIFO buffer size chosen based on design criteria such as packet size and link transfer rates. It is respectfully submitted that Bastiani does **not** disclose or suggest providing a **comparator that outputs a logic level of 1 for indicating that at least one error flag is set in the data words stored in memory.**

Applicants' admitted prior art (APA) refers to a dual 16 word FIFO asynchronous circuit. Applicants' APA does **not**, however, provide a comparator that compares a value of an error write counter with a value of an error read counter. Applicants' APA does **not** provide a comparator that outputs a logic level of 0 when the value of the error write counter is coincident with the value of the error read counter. Applicants' APA does **not** suggest providing a logic level 1 by the comparator to indicate that at least one error flag is set in the words stored in memory.

Amended claim 1 is not obvious in view of the cited references. Favorable reconsideration is requested for amended claim 1.

Although not the same, claims 2, 4 and 5 have been amended to include features similar to amended claim 1. Claims 2,4 and 5 are, therefore, not subject to rejection in view of the cited references for the same reasons set forth for amended claim 1.

Dependent claims 3 and 6 depend, respectively, from claims 1-2 and claims 4-5 and are, therefore, not subject to rejection in view of the cited references for at least the same reasons set forth for amended claim 1. Favorable reconsideration is requested.

Conclusion

Claims 1-6 are in condition for allowance.

Respectfully submitted,

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Attachments: Figures 9 and 10 (2 sheets)
Abstract

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The Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

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January 26, 2004 Fran Petrillo